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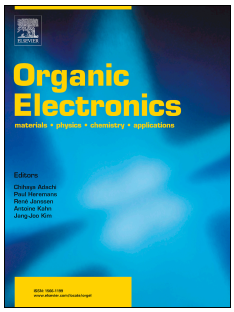

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PII: S1566-1199(19)30016-3

DOI: https://doi.org/10.1016/j.orgel.2019.01.010

Reference: ORGELE 5061

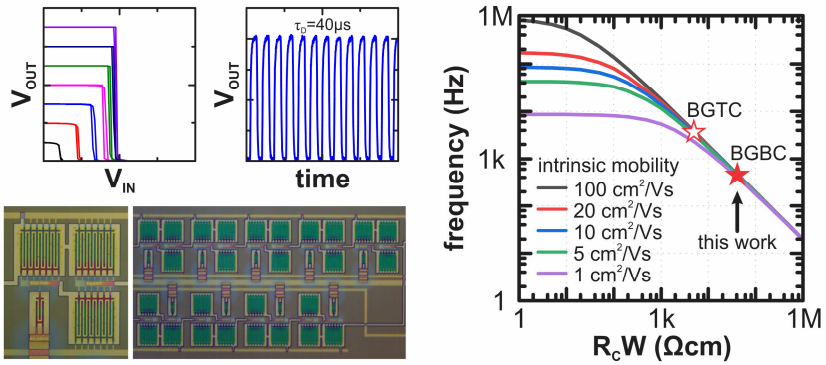
To appear in: *Organic Electronics*

Received Date: 12 September 2018

Revised Date: 7 January 2019

Accepted Date: 8 January 2019

Please cite this article as: R. Janneck, T.S. Nowack, F. De Roose, H. Ali, W. Dehaene, P. Heremans, J. Genoe, C. Rolin, Integration of highly crystalline C8-BTBT thin-films into simple logic gates and circuits, *Organic Electronics* (2019), doi: https://doi.org/10.1016/j.orgel.2019.01.010.



Article type: Full Paper

Integration of Highly Crystalline C8-BTBT Thin-Films into Simple Logic Gates and Circuits

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Keywords: organic semiconductors; single crystal; contact resistance; photolithography; ring oscillator

ABSTRACT

Highly crystalline organic thin films possess the charge carrier mobilities needed for high-performance, low-cost flexible electronics. However, only few reports exist that show the integration of these films into short-channel organic circuits. This work describes the integration of highly crystalline layers of the thermally and chemically fragile small molecule C_8-BTBT. Thin films of this material are processed by a combination of zone-casting and homoepitaxial vacuum evaporation and display an average charge carrier mobility of 7.5 cm^2/Vs in long channel transistors. The integration of these films into a circuit technology based on a 5 µm channel-length bottom-gate bottom-contact transistor topology results in inverters with gains up to 40 as well as a robust 19-stage ring oscillator. This circuit requires the simultaneous operation of 80 TFTs and displays a stage delay of 40 µs, resulting in an operating frequency of 630 Hz at an operating voltage of 10 V. With the help of circuit modelling, we quantify the relationship between the speed of ring oscillators and the contact resistance of individual transistors. Indeed, the successful integration of highly-crystalline layers with high intrinsic mobility stresses the need for advances in contact engineering.

1. INTRODUCTION

Organic thin film transistors (TFTs) are widely studied as potential candidates for next generation flexible, large area electronics[1–5]. Especially their good p-type conductivity makes them a promising match with n-type-only metal-oxide TFTs for flexible integrated circuits[6,7]. Recent advances in molecular design and fabrication techniques have led to mobilities in the range of 10 cm^2/Vs[8–12], similar to amorphous metal-oxide semiconductors such as indium-gallium-

zinc-oxide (IGZO)[7,13]. Improved fabrication techniques typically target enhanced order in the organic thin films [10,12,14–19]. The resulting films display excellent crystallinity and high intrinsic charge carrier mobility. However, most of these efforts have utilized long channel transistors for electrical characterization in order to avoid adverse contact effects on the thin film mobility extraction[20,21]. Yet, as recently reminded by Klauk[22], the full exploitation of these highly performing thin films into devices operated at high frequency requires downscaling of the channel length. Only very few reports combine the benefits of highly crystalline thin films with the advantages of short channel lengths and demonstrate high frequency operation[23,24]. One major reason for this deficiency stems from the fragile nature of organic semiconductors, which are easily destroyed by conventional photolithography[25]. Although several orthogonal photoresist systems have been proposed to achieve photolithographic patterning of the fragile organic layer without degradation [23–29], these have seldom been demonstrated on highly crystalline thin films of organic semiconductors for circuit applications.

Here, we developed a process flow to integrate highly crystalline organic thin films of C_8-BTBT. This material was chosen as a benchmark due to its commercial availability and its well-studied properties, including high reported intrinsic charge carrier mobilities[12,30,31]. Moreover, C_8-BTBT thin films are notoriously fragile, both chemically and thermally, making their integration a challenge which further validates our approach. The films are fabricated by our recently developed lateral homo-epitaxial growth method that combines zone-casting and evaporation in high-vacuum to deliver highly uniform thin films with cm-long single-crystalline domains[12]. These films are then patterned while retaining their morphology and electrical performance. We integrate these films in a fully patterned process flow, demonstrating working inverters and 19-stage ring oscillators. The inverters reached gains up to 40 with good yield and reproducibility. The ring oscillator achieved a stable operating frequency of 630 Hz at an operating voltage of 10 V, corresponding to a stage delay of 40 μs. We show that the frequency is limited by the contact resistance inherent to the system.

2. EXPERIMENTAL SECTION

2.1. Integration of highly crystalline organic thin films

As detailed in the Results section, different types of substrates were used throughout this study. Prior to organic semiconductor layer growth, all substrates were cleaned sequentially in heated ultra-sonic baths of detergent, de-ionized water, acetone and isopropanol. After a 15’ UV/ozone treatment, the substrate surfaces were immediately modified with adequate self-assembled monolayer treatment(s) that ensure proper wetting during zone-casting and passivates the

dielectric surface to ensure good electrical characteristics[32]. C_8-BTBT (2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene) was supplied by Sigma Aldrich and purified prior to usage in a tri-zone purification oven. Solutions were prepared in anhydrous heptane (from Sigma Aldrich, 99%). The solution coatings were performed using a home-built zone-casting setup as previously described[33]. All experiments were done at room temperature at a coating speed of 20 μm/s. Afterwards, additional 50 nm C_8-BTBT was thermally evaporated in an ultra-high vacuum chamber at a deposition rate of 0.2 Å/s and substrate temperature of 22°C to achieve a closed, highly crystalline thin film as previously described[12]. Subsequently, photolithographic patterning was done using a non-fluorinated, chemically amplified, i-line photoresist system[29]. Oxygen plasma reactive ion etching was used to remove the exposed organic thin film. The active area of the organic thin film is protected by the photoresist system during this step. Afterwards, the remaining photoresist is stripped from the sample.

For easy electrical characterization of the thin films, we used common-bottom-gate/top-contact transistors based on 3x3 cm highly doped silicon substrates with a 170-nm thick thermally grown SiO_2, resulting in a capacitance of C_i = 20.3 nF/cm^2 (see Figure S1a-f for schematic). After substrate cleaning, the SiO_2 was modified by exposure to a vapor of phenethyl(trichloro)silane (PETS; from Sigma Aldrich, 98%) for 1h in a vacuum oven heated at 140°C. The C_8-BTBT thin film was deposited as described in the previous section. Subsequently, source and drain contacts were deposited by vacuum evaporation through a shadow mask. For contacts, 6 nm 2,2'-(perfluoronaphthalene-2,6-diylidene)dimalononitrile (F_6-TCNNQ) and 50 nm gold were deposited at a deposition rate of 0.2 Å/s and 1 Å/s, respectively. The transistor channel width was 2035 μm, while the channel length varied between 200 μm and 40 μm. The channel was aligned in the coating direction, so that the initial zone-cast ribbons fully bridge the gap between the source and drain contacts. To ensure good electrical characteristics[20,21], the samples were annealed in a nitrogen-filled glove box at a mild temperature of 50°C for 10 hours. Afterwards, the individual transistors were patterned by photolithography as described in the previous section. Reference devices were separated by scratching the organic film with a thin needle to create islands of similar shape as the islands defined by photolithography. A total of 320 TFTs were fabricated and measured per sample which includes 40 TFTs for each channel length.

2.2. Integrated devices: transistor, inverters and ring oscillators

Integrated devices were fabricated on 3x3 cm^2 silicon substrates using a metal/insulator/metal stack defined by conventional photolithography[34] (see Figure S1g-l for schematic). After substrate cleaning, the gate electrode (2 nm Ti/ 100 nm Au) was thermally-evaporated and patterned by lift-off. Afterwards, a 100-nm thick Al_2O_3 layer was deposited by

atomic layer deposition and serves as the gate dielectric with a capacitance of C_i = 80.3 nF/cm^2. After patterning vias through the dielectric by wet-etching, the source and drain electrodes (5 nm MoO_x/ 30 nm Au) were deposited and patterned by lift-off. The integrated transistor channel width was 420 μm, while the channel length varied between 100 μm and 2 μm. Channel lengths for all the transistors in inverters are 5 μm. The channel width for the inverters using the pseudo-CMOS diode-load design are T_1: 155 μm, T_2: 1474 μm, the pull-up and pull-down transistors have the same dimensions T_{PU}=T_{PD}: 1474 μm. In the pseudo-CMOS zero-V_{GS}-load design the dimension of T_1 and T_2 are inversed. The same dimensions are used in the ring oscillators. After cleaning and UV ozone treatment of the substrates, we first treated the Au electrodes with 2,3,4,5,6-Pentafluorothiophenol (PFBT) (from Sigma Aldrich, 97%) to improve charge injection[35,36] and wetting behavior during zone-casting[32]. Afterwards, the Al_2O_3 dielectric was treated with n-Tetradecylphosphonic acid (from Sigma Aldrich, 97%). Finally, the organic thin film was deposited and patterned as previously described. The zone casting direction was aligned with the channel directions, so that the initial zone-cast ribbons fully bridge the gap between the source and drain contacts. A full description of the fabrication flow for the integrated devices and circuits is given in Table S1 in the Supporting Information.

2.3. Morphology and electrical characterization

Light microscope images were obtained using an Olympus AX70 microscope in reflected light. AFM studies were done with a Bruker dimension edge scanning probe in tapping mode. Electrical characterization of the individual TFTs and the inverters were done using an Agilent Agt1500 in dry air. Field-effect mobilities were evaluated in the saturation regime using the conventional transconductance analysis given by $\mu_{eff,sat} = (2L/W)(1/C_i)\left(\partial\sqrt{I_D}/\partial V_G\right)^2$, where C_i is the gate capacitance per unit area. Threshold voltages are obtained by the intercept of the slope of the current $I_D^{1/2}$, taken at the region of the mobility plateau, with the gate voltage axis. Saturation measurements of the top-contact transistors were done on the common gate devices at a drain voltage of V_D = -40 V while sweeping the gate voltage from V_G = 10 V to V_G = -40 V, while the bottom-contact transistors were measured a drain voltage of V_D = -20 V while sweeping the gate voltage from V_G = 20 V to V_G = -20 V. Contact resistance measurements were done in the linear regime at a drain voltage of V_D = -1 V. Electrical characterization of the ring oscillators were done using an Agilent 4156C in ambient air. The oscillation was measured using a picoprobe 34A from GGB Industries and an Agilent DSO6102A oscilloscope. The measurements were performed at V_{DD} = 5 V and V_{SS} = -V_{DD} = -5 V.

3. RESULTS AND DISCUSSION

3.1. Integration of highly crystalline organic thin films

The patterning of the organic semiconductor is mandatory to ensure good electrical isolation and thereby avoid leakage currents that appear as high Off-currents in the TFT characteristics. First, we optimized the photolithographic patterning process of highly crystalline organic layers. We achieved patterned structures with very sharp edges that perfectly preserve the film morphology in the areas protected by the resist and entirely remove it in the unprotected areas (Figure 1a). The minimum feature size is around 3 µm as shown in Figure 1b and c. This means that we can pattern the C_8-BTBT layer down to island sizes of few micrometer. This resolution is sufficient to integrate organic thin films into state of the art inverters and ring oscillators which only require semiconductor islands in the range of few tens of micrometer.

Figure 1 Patterned C_8-BTBT films. (a) AFM image of the edge of a large structure showing a sharp feature edge. (b) AFM image of the smallest patterned structure sizes. (c) Topography along the black line of (b) showing patterning line widths of 3 µm. Inset shows the molecular structure of C_8-BTBT.

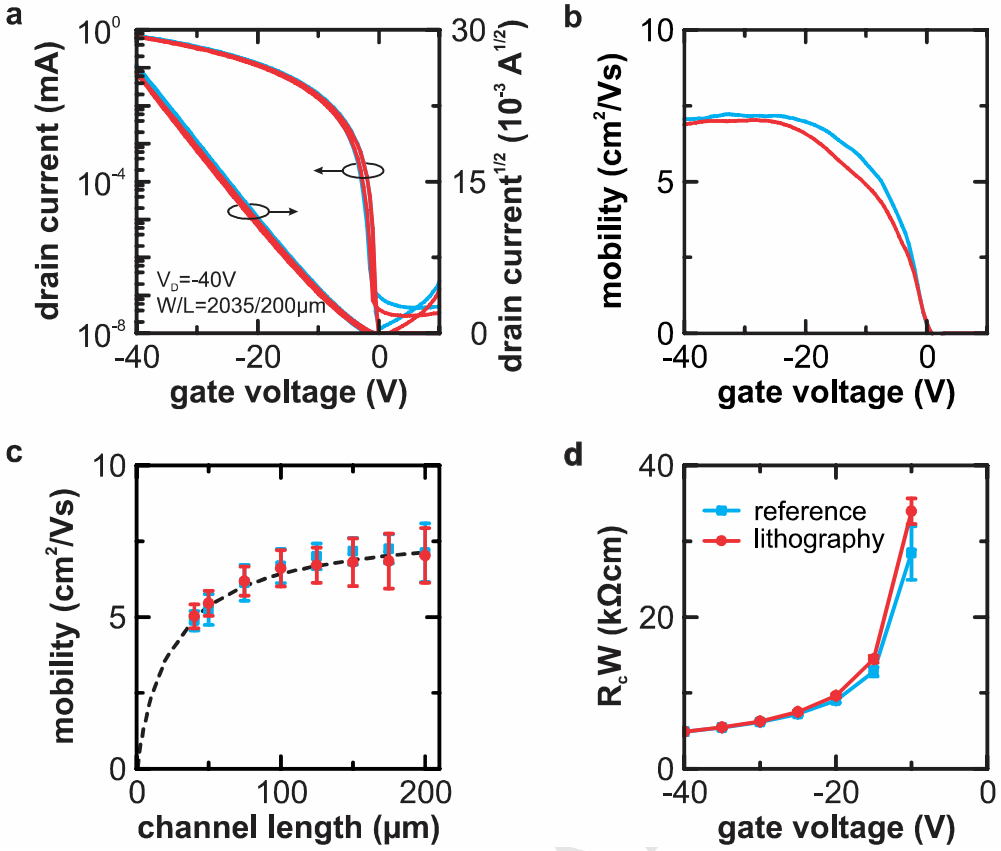
To investigate the impact of photolithographic patterning on the electrical performance of the highly-crystalline organic films, we fabricated bottom-gate/top-contact thin film transistors. The process flow of the fabrication is schematically shown in Figure S1a-f. After the deposition of the highly crystalline C_8-BTBT organic thin film on the complete substrate using the lateral homo-epitaxial growth method[12], we deposit the source and drain electrodes by vacuum evaporation through shadow masks (Figure S1b). Depositing the electrodes ensures an easy fabrication process, but limits the channel length of the transistor to 40 µm. The photoresist is then deposited, exposed and developed (Figure S1c, d). After the etching of the unprotected organic thin film layer and the subsequent stripping of the remaining photoresist (Figure S1e, f), we obtain individual transistors with photolithographically patterned organic thin film islands. In order to assess the influence of the

photolithographic steps on the electrical performance, reference samples were also fabricated in parallel but with organic thin film islands patterned by scratching with a thin needle. Note that depositing the electrodes before patterning the organic film ensures that the semiconductor-electrode interface is not influenced by the patterning process. Moreover, this yields the best alignment precision since photomasks are aligned by a high-precision system while the shadow masks are aligned by hand.

Figure 2 compares typical electrical characteristics of the photolithographically patterned thin film transistors with reference devices. We achieved almost identical average device performance for the samples that underwent the photolithographic patterning process as for the reference samples. The photolithographic patterning process is benign to the organic thin film, despite the high fragility of C_8-BTBT thin films to processing conditions. For long channel length devices (L = 200 µm), we obtain well-behaved transfer characteristics with high on-off ratios (>10^7), on-set and threshold voltages around 0 V and -5V respectively and small hysteresis (Figure 2a). The effective mobility in the saturation regime shows a broad mobility plateau at 7.5 cm^2/Vs over a large gate voltage range (Figure 2b), which indicates minimal non-linear contact effects and validates the use of gradual channel approximation for mobility extraction[20,21,37]. Upon decreasing channel lengths L, the effective mobility lowers down to 5 cm^2/Vs at L = 40µm, due to the increased weight of contact resistance (Figure 1c). The evolution of effective mobility μ_{eff} with channel length is fit by:

$$\mu_{eff} = \frac{\mu_{int}}{1+\frac{L_{1/2}}{L}} \quad (1)$$

where μ_{int} is the intrinsic mobility of the thin film semiconductor without detrimental contact effects, and $L_{1/2}$ is the channel length below which contact resistance dominates over channel resistance[31,38,39]. The fit in Figure 2c delivers μ_{int} = 8.1 cm^2/Vs and $L_{1/2}$ = 25 µm. This relation is also useful to extrapolate the effective mobility to channel lengths lower than what can be achieved in practice with shadow mask patterning: At channel lengths of 5 µm, we would only obtain effective mobilities of about 1.4 cm^2/Vs.



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194 **Figure 2** Comparison of typical electrical characteristics for C_8-BTBT films patterned by
195 photolithography and scratched reference devices. No obvious difference is observed between
196 lithographically patterned and reference devices. (a) Transfer curves in saturation and (b) the
197 corresponding mobility versus gate voltage curves. (c) Extracted saturation mobility as a function of
198 channel length. (d) Contact resistance R_CW extracted by the transfer line method, reaching values
199 around 5 kΩcm. Each data point in (c) and (d) corresponds to the average value and spread of the
200 measured 40 devices for each channel length.

201

202 The mobility drop in lower channel length and the relatively long $L_{1/2}$ indicates that contact
203 resistance affects the shortest devices despite the doped F_6-TCNNQ interlayer between the organic
204 semiconductor and the gold contact. The contact resistances is extracted using the transfer length
205 method (Figure 2d). It is minimal (~5 kΩcm) at the highest gate voltage V_G = -40V and then
206 typically increases with smaller $|V_G|$. These contact resistances values are among the lowest
207 published for C_8-BTBT[35,40,41]. Only very thin films might be able to further reduce the contact
208 resistance for top-contact devices[42]. As for the transfer curves, the contact resistance remains
209 unaffected by the patterning process: The photolithography does not cause damage to the
210 semiconductor/electrode interface. As this patterning process preserves both the organic thin film
211 and the contacts, then it also preserves the evolution of effective mobility with channel lengths in
212 Figure 2c. The device to device reproducibility is excellent, enabling the integration of these
213 devices into more complex circuits [43].

3.2. Integrated transistors

In this section, the optimized highly crystalline C_8-BTBT thin films described so far are integrated into a circuit technology. The most straightforward integrated transistor topology is a bottom-gate/bottom-contact architecture whose metal/insulator/metal stack is patterned by photolithography prior to the deposition and patterning of the fragile organic thin film. This coplanar transistor architecture is far easier to fabricate, but it also usually results in inferior electrical characteristics when compared to the staggered architectures, due to its lower charge transfer area and its difficult doping of the contacts[44,45]. To somewhat alleviate these issues, we chose a combination of MoO_x and Au for the source/drain electrodes as they have been shown to result in increased carrier injection for p-type semiconductors, leading to lower contact resistances, smaller threshold voltages and higher effective mobilities[40,46]. The simple fabrication of the bottom-gate-bottom contact topology enables high yield. For example, its past implementation with pentacene has already delivered fully operational, large and complex circuits (microprocessor with 3381 OTFTs)[47]. This topology therefore remains a viable route for integration of circuits with large transistor count.

Figure 3 shows the electrical characteristics of the fully photolithographically patterned bottom-gate/bottom-contact transistors with highly-crystalline organic semiconductor. We achieve a good switching behavior with high on-off ratios ($>10^7$) and onset voltages close to 0V in Figure 3a. The mobility curves in Fig. 3b for long (100 µm) and short (5 µm) channel devices can be directly compared to the mobility curves of the top contact device in Fig. 2b. This reveals a mobility loss and a deepening of the threshold. This performance loss upon integration and downscaling is a direct consequence of the higher contact resistance in the bottom-contact topology: it is about an order of magnitude higher than for the top-contact architecture (Figure 3d), reaching values of 40 kΩcm at the highest gate voltage.

Figure 3d also shows the channel resistance calculated for the intrinsic mobility of μ_{int} = 7.5 cm^2/Vs measured in the previous section. Thanks to this high mobility, the channel resistance of short channel bottom contact is well below the contact resistance. In consequence, downscaling these high-mobility devices only marginally improves the on-current of the transistors, as the total resistance of the transistor is fully dominated by the contact resistance. For example, scaling the channel length by a factor 20 in Figure 3a only brings a two-fold increase in on current. In consequence, the effective mobility extracted for these devices in Figure 3b using the standard gradual channel approximation model has a severe channel length dependence and does not show a clean broad plateau region above threshold. This model is ill-suited to fit transfer curves of contact dominated thin film transistors[20,21]. Yet, we fit in Figure 3c the channel dependence of the

effective mobility using Equation 1 with μ_{int} = 4.7 cm^2/Vs and $L_{1/2}$ = 85 µm. As channels shorter than $L_{1/2}$ are dominated by contact, this confirms that ~98% of the resistance of the 5 µm long channel is encountered at the contacts. Indeed, contact resistance takes a very high toll in downscaled transistors based on highly crystalline films with high mobility. Unfortunately, improving charge injection in the bottom contact configuration is a challenge as it is difficult to propose contact-doping strategies that do not contaminate the semiconductor-dielectric interface or perturb the film growth.

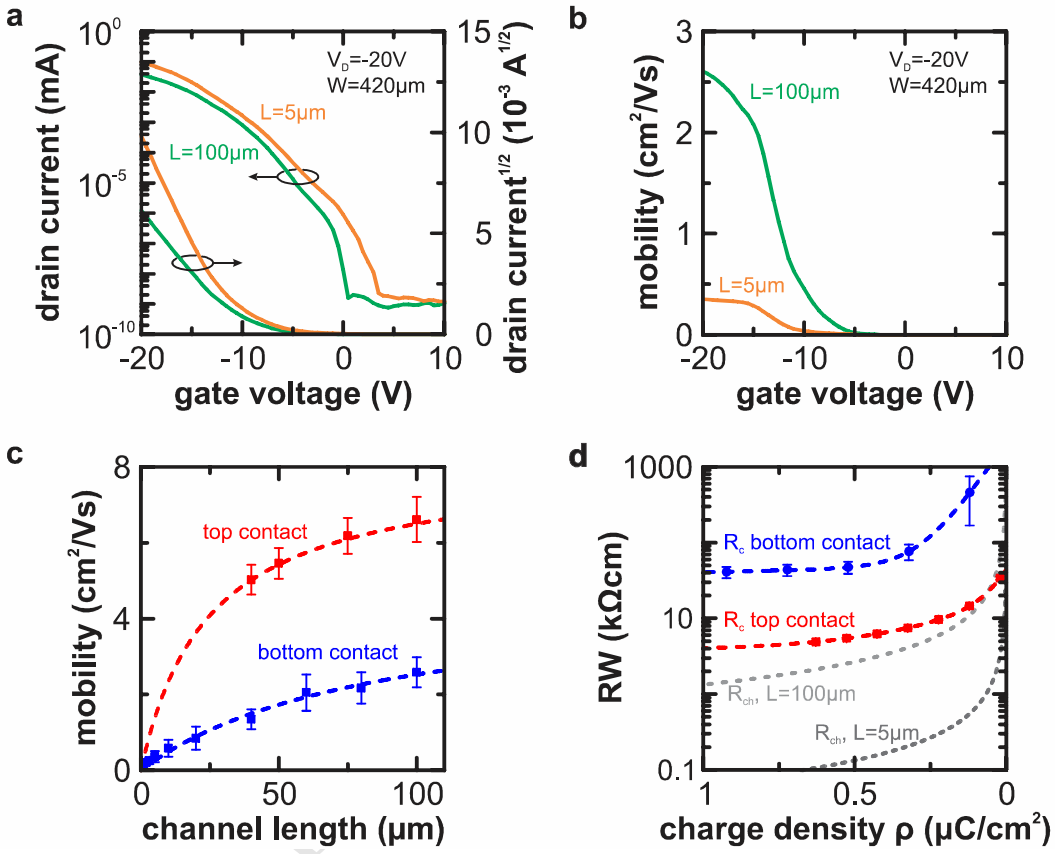

Figure 3 Electrical results of fully integrated bottom-contact transistors. (a) Transfer curves in saturation and (b) the corresponding mobility versus gate voltage curves for short channel and long channel devices. The channel length only has a marginal influence on the current, as the device is severely contact limited. (c) Effective saturation mobility as a function of channel length. (d) Estimated contact resistance R_CW as extracted from the TLM measurements, reaching values around 40 kΩcm for the bottom contact-devices. R_CW is plotted as a function of charge density to allow comparison of the top and bottom contact topologies despite different insulators.

3.3. Integrated inverters

Despite the high price paid to contacts in individual transistors, we pursued their integration into circuits. Complex digital electronic circuits are usually built up from large amounts of logic gates, the simplest of which are inverters. The gain and noise margin extracted from inverter

characteristics are useful to quantify the robustness of the digital circuit to transistor parameter variations[43]. The two most common inverter designs in the literature are the zero-V_{GS}-load and the diode-load. The advantage of the zero-V_{GS}-load logic is its high noise margin and therefore large circuit robustness, but it requires normally-on devices, that is a positive onset-voltage V_{on} in p-type logic. The advantage of the diode-load logic is its superior operation speed, but it requires smaller variations during the fabrication process due to its smaller noise margin. To reduce the variations from the thin film fabrication flow, we are using our previously developed lateral homo-epitaxial fabriation technique to fabricate highly crystalline thin films with small device-to-device variations (<10%)[12]. Moreover, we employ pseudo-CMOS logic as it shifts the trip voltage towards the middle of the supply rail. This guarantees a high gain and noise margin, hence a robust technology with higher noise immunity for realizing large scale digital circuits[7,48]. But it comes at the expense of a supplementary power supply rail; slower operation and a higher footprint. We fabricated both the pseudo-CMOS zero-V_{GS}-load (Figure 4a) and pseudo-CMOS diode-load (Figure 4d) inverters, and compare their electrical characteristics. As in our previous work[6], critical dimensions used for mimimal line widths, overlay accuracy, line seperation etc. are defined by the photolithographic patterning step and are chosen to be 5 µm. The channel lengths were therefore also chosen to be 5 µm for all the transistors employed in the inverters and ring oscillators.

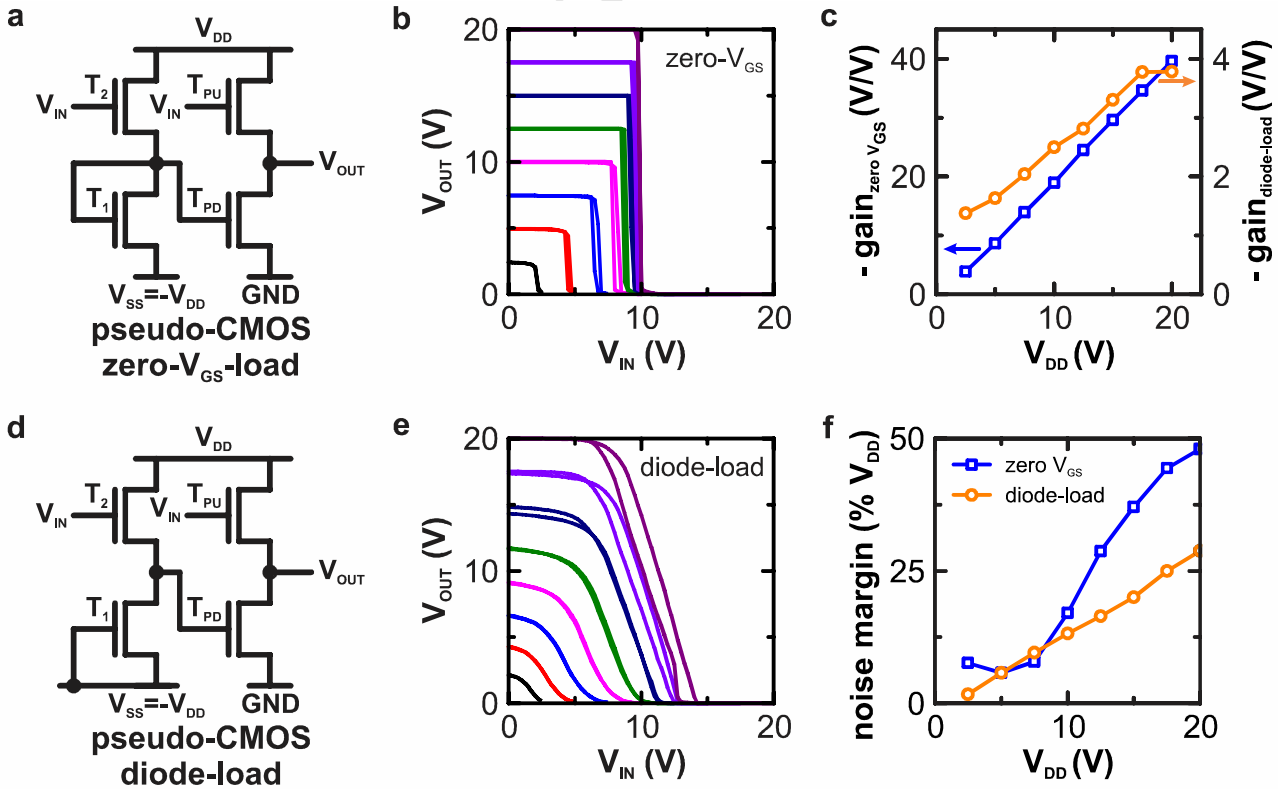

Figure 4 Inverter circuit design and measurements. (a) p-type pseudo-CMOS zero-V_{GS}-load circuit design and (b) the measured inverter curves of this design. (d) p-type pseudo-CMOS diode-load

circuit design and (e) the measured inverter curves of this design. (c) Small-signal voltage gain and (f) noise margin of both inverter designs as a function of the supply voltage V_{DD}.

Figure 4b and e show the output voltage (V_{OUT}) vs. input voltage (V_{IN}) characteristics for both the pseudo-CMOS zero-V_{GS}-load and pseudo-CMOS diode-load logic, respectively. Both designs show a good rail-to-rail voltage inversion with trip voltages close to the middle of the supply rail, especially for higher operating voltages V_{DD} and V_{SS}. Moreover, both designs already operate at low voltages V_{DD} = 2.5V. This is especially remarkable considering the not so high capacitance of the gate dielectric and the low transistor threshold voltages. As expected, the pseudo-CMOS zero-V_{GS}-load design shows very steep switching from high to low output voltages. This results in small-signal voltage gains up to 40 in Figure 4c. The small signal voltage gain is probably limited by the measurement resolution rather than its intrinsic performance, as we only measured at step sizes of 0.25 V. This high gain combined with the trip voltage close to the middle of the power rail results in high noise margins up to 48% of V_{DD} (Figure 4f), which is close to the maximum possible noise margin of 50%. The pseudo-CMOS diode-load design delivers gains that are one order of magnitude lower than their zero-V_{GS} counterpart. Nevertheless, the trip voltage is also close to the middle of the supply rail and therefore this logic also achieves very good noise margins of up to 29% of V_{DD}. Note that using a pseudo-CMOS logic, the theoretical noise margin limit is only half of that of conventional logic. According to this definition, our relative noise margins are in fact only half as well, reaching values up to 24% and 14.5% of the supply voltage for the pseudo-CMOS zero-V_{GS} and diode-load logic, respectively.

3.4. Integrated circuits

We used the same peudo-CMOS inverter structures in a 19-stage ring oscillator configuration. As schematically shown in Figure 5d, an additional inverter stage is added after the actual ring oscillator in order to reduce the load of the needle probe and therefore avoid influencing the oscillation speed. With 4 transistors per stage, the 19-stage ring oscillators uses a total of 80 transistors. Note that most ring oscillators in the organic thin film transistor literature employ fewer stages and therefore fewer transistors. Indeed, large ring-oscillators are more difficult to produce as circuit yield decreases with increasing amount of stages[43]. Larger oscillators, however, constitute a better benchmark to evaluate the ability of an integrated technology to deliver larger circuits[49]. Figure 5a-c show optical images of a pseudo-CMOS diode-load ring oscillator structure. The zone casting was performed perpendicular to the fingers of the interdigitated source and drain electrodes. As seen previously[32], the bottom-contact electrodes have no influence on the film formation during the coating process: Continous single-crystalline ribbons of C_8-BTBT completly bridge the channel between the interdigitated fingers. The darker flakes on top of the ribbons in Figure 5c are

due to non-eptixial grains that form during regrowth on top of the single crystalline ribbons and do not impact charge transport at the interface with the dielectric. Finally, these pictures also show that the photolithographic patterning of the organic thin film is clean, leaving no defects or residues.

With the pseudo-CMOS diode-load design, we achieved a stable operation frequency around 630 Hz, corresponding to a stage delay of 40 µs, at a voltage of V_{DD} = 5 V, (Figure 5e). Like the inverters, the ring oscillator already shows stable operation at V_{DD} = 2.5 V with an oscillating frequency of 180 Hz, corresponding to a stage delay of 140 µs. In the pseudo-CMOS design, the actual operating voltage is the difference between V_{DD} and V_{SS}, thus, for comparison with standard designs, the operating voltage of pseudo-CMOS ring oscillators is always twice the V_{DD}. The pseudo-CMOS zero-V_{GS}-load design resulted in operating frequencies of 20 Hz that do not significantly increase with increasing V_{DD}. Although the inverters of this design show higher static performance in Figure 4c and f, the dynamic performance of the pseudo-CMOS zero-V_{GS}-load logic is much lower due to the large capacitance at the output node. Moreover, the zero-V_{GS}-load design requires normally on transistors (V_{on} > 0V), but in our case, the transistors are normally off (V_{on} < 0V) which further decreases the speed of the pseudo-CMOS zero-V_{GS}-load logic.

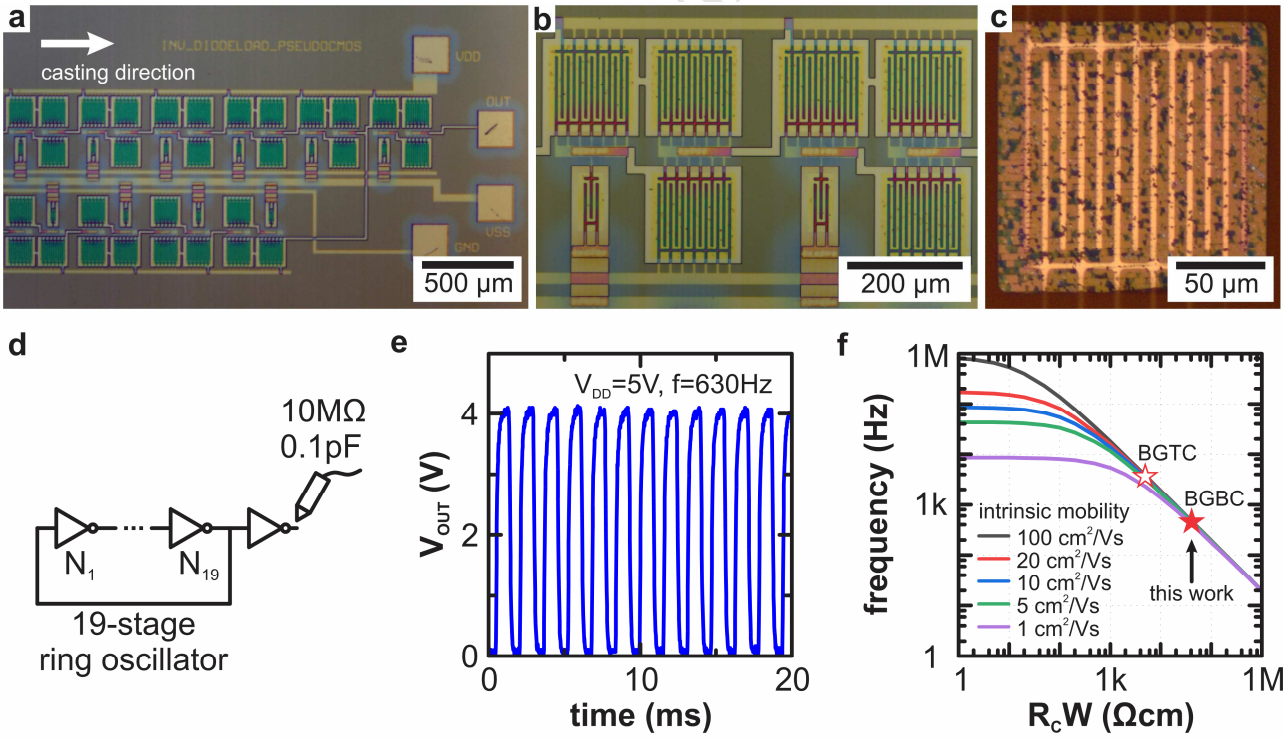

Figure 5 Fully patterned ring oscillators. (a), (b) bright field microscope images, (c) polarized light microscopy image. (d) Schematic of the measurement setup. (e) Measured signal output of the ring oscillator, resulting in an oscillating frequency of 630Hz. (f) Simulated dependency of the ring oscillator frequency on the intrinsic charge carrier mobility and contact resistance R_CW. BGBC are

the bottom-gate/bottom-contact devices used in this study. BGTC shows what would be possible with the extracted contact resistance for bottom-gate/top-contact devices.

While we were able to obtain well-behaved robust large-scale ring oscillators at low operating voltages, the resulting operating frequency remains an orders of magnitude lower than what has been previously achieved[34]. This is not necessarily expected, considering the high intrinsic mobility of our highly crystalline C_8-BTBT thin films. The slower operation of our devices is partially due to the choice of the slower pseudo-CMOS design. The contact resistance also plays an important role in limiting the frequency. Indeed, when assuming a mobility of μ = 7.5 cm^2/Vs and a threshold voltage of V_{th} = -1V, simple SPICE simulations predict operating frequencies around 65 kHz for the exact same geometry and operating voltages as our actual pseudo-CMOS diode load 19-stage ring oscillator. Hence, the real oscillator operates around 2 orders of magnitude slower than ideally expected. The simulation already takes all the geometric parasitics, e.g. due to the overlap capacitance, into account. Therefore, the main cause for lower oscillating frequency is the lower effective mobility due to contact resistance. The effective mobility can be calculated from the intrinsic mobility μ_{int} and the contact resistance R_c by:

$$\mu_{eff} = \mu_{int} \frac{1}{1+\frac{\mu_{int}}{L} R_C W C_i (V_G - V_{th} - V_{DS})} \quad (2)$$

where C_i is the gate-dielectric capacitance, V_{th} *is* the threshold voltage and V_G and V_{DS} are the applied gate and drain voltage, respectively[50]. During ring-oscillator operation, the T1 transistor with W/L = 155 µm/5 µm is the speed-defining device. It approximately reaches its highest current when biased with $V_G = V_{DD}$ and $V_{DS} = V_{DD}/2$. Using Equation 2, the effective mobility of that device is in the range of μ_{eff} = 0.075 cm^2/Vs, that is 2 orders of magnitude smaller than the mobility of the long channel, top-contact devices in Figure 2b. Similar observations were already seen in the single transistor bottom-contact devices. Clearly, this reduced effective mobility of the bottom-gate/bottom-contact integrated transistors is responsible for the rather slow ring oscillator operation. To achieve higher operating frequencies with the same geometry, one would have to significantly reduce the contact resistance by e.g. moving to a staggered transistor architecture, which poses serious integration challenges.

We further elaborated the SPICE model of the pseudo-CMOS diode load 19-stage ring oscillator in order to fully assess the impact of contact resistance on circuit operation. In the model, we added additional resistors to every transistor to simulate the effect of contact resistance. The simulation, shown in Figure 5f, further confirms that the operating frequency is criticially dependent on the contact resistance. Two regions of operation are shown in the figure, separated by

a threshold contact resistance value. Below threshold, at very low contact resistance (e.g. R_cW ~ 1 Ωcm), the contact resistance is still small compared to the channel resistance and frequency shows a slow linear decrease with RcW. Also, in this plateau region, the frequency scales linearly with the intrinsic charge carrier mobility of the thin film μ_{int}, as expected from theory. Above the threshold, however, the operating freqency exponentially decreases with increasing contact resistances resulting in a very sharp circuit speed drop. The value of the threshold becomes lower as the intrinsic mobility increases, since devices using higher mobility thin films are more sensitive to contact effects. For example, in an oscillator based on a semiconductor with μ_{int} = 10 cm^2/Vs, the expontential loss of frequency starts from R_cW = 100 Ωcm onwards. As a result, all frequency vs. contact resistance characteristics fall onto each other once the contact resistance reaches typical values observed in integrated organic thin film transistor of a few kΩcm[31]. Hence, the intrinsic mobility of the organic semiconductor film has only a marginal effect on the expected ring oscillator frequency. The simulation of our ring oscillator predicts a frequency around 500 Hz for the contact resistance extracted for our bottom-contact devices (R_cW = 40 kΩcm at V_G = -V_{DD}). This fits very well the actual measured value of 630 Hz (plain star symbol in Figure 5f).

As seen in the comparison between the transfer length measurements of staggered and coplanar (Figure 3d) transistor topologies, the integration of a bottom-gate/top-contact transistor could reduce the contact resistance by about an order of magnitude and therefore increase the operating frequency by a similar factor, provided that capacitive coupling between gate and source/drain electrodes is maintained at the same level (hollow star symbol in Figure 5f). Even such contact resistance in the range of few kΩcm remains too high to take advantage of the enhanced mobility of highly crystalline organic semiconductor films. In reality, exploiting the full potential of these films would require contact resistance values smaller than 100 Ωcm, which is in the range of the best values published in the field for simple, non-integrated devices[17,20]. Clearly, high-mobility semiconductors do not present a clear gain for integrated circuit applications, unless they are accompanied by improvements in charge injection and extraction between the source/drain electrodes and the semiconductor film[22].

This analysis is based on transistors with 5 µm channel lengths. Moving to smaller channel lengths puts even stronger requirements on the contact resistance as this shifts the contact resistance threshold to exponential frequency loss towards lower and lower values (see Figure S2). Even with record contact resistances of a few tens of Ωcm, the speed gain conferred by smaller channel lengths is negligible. Figure S2 nevertheless reveals that the operating frequency still increases in the same proportion as the channel length decreases. This frequency gain is solely due to the lower

parasitic capacitances in the downscaled architecture, since in our model, all transistor dimensions are scaled with the same proportions.

4. SUMMARY

In this work, we discussed the integration of highly-crystalline, high-performance thin films of an organic semiconductor, C_8-BTBT, into simple logic gates and circuits. The C_8-BTBT is processed by zone-casting followed by an homoepitaxial regrowth by vacuum evaporation, which delivers high quality thin films with mm-long single crystal domains and an intrinsic charge carrier mobility of 7.5 cm^2/Vs. The patterning of such films using an orthogonal photolithography process is well-suited for integration since it results in sharp patterns with no damage to the film morphology or its electrical performance. We therefore fabricated organic transistors, inverters and ring oscillators based on a bottom-gate/bottom-contact architecture with a channel length of 5 µm.

This integration inevitably leads to an elevation in contact resistance (in the range of 40 kΩcm) and a corollary loss in effective mobility down to 0.1 cm^2/Vs. Nevertheless, thanks to the pseudo-CMOS architecture, the inverters show well-behaved voltage curves with full rail-to-rail switching, small-signal gains as high as 40 and noise margins close to the theoretical optimum. Furthermore, we successfully fabricated 19-stage ring oscillators based on 80 transistors with the photolithographically patterned highly crystalline C_8-BTBT film. The oscillators reach frequencies around 600 Hz, corresponding to a stage delay of 40 µs, at a supply voltage of $V_{DD} = -V_{SS} = 5V$. Our circuit simulations clearly show that the contact resistance is the limiting factor in the ring oscillators and cancel the gains expected from the use of a high-performance semiconductor film. Any effort aiming at the integration of OTFTs necessitates to match improvements in charge carrier mobility of the semiconductor with improvements in the contact resistance of transistors. No gain will be obtained from a mobility improvement only.

SUPPLEMENTARY INFORMATION

Supplementary information related to this article can be found at...

ACKNOWLEDGEMENTS

We acknowledge funding from the European Research Council under the European Seventh Framework Programme (FP7/2007-2013) / ERC grant agreement nº320680 (EPOS CRYSTALLI) and from the Research Foundation Flanders (FWO Vlaanderen) under the FWO-ARRS research

collaboration program / grant number G0B5914N (ORSIC-HIMA). F. De Roose thanks the Agency for Innovation by Science and Technology in Flanders (IWT-Vlaanderen) for financial support. We would like to thank Nippon Kayaku Co. for supplying the C_8-BTBT used in this study.

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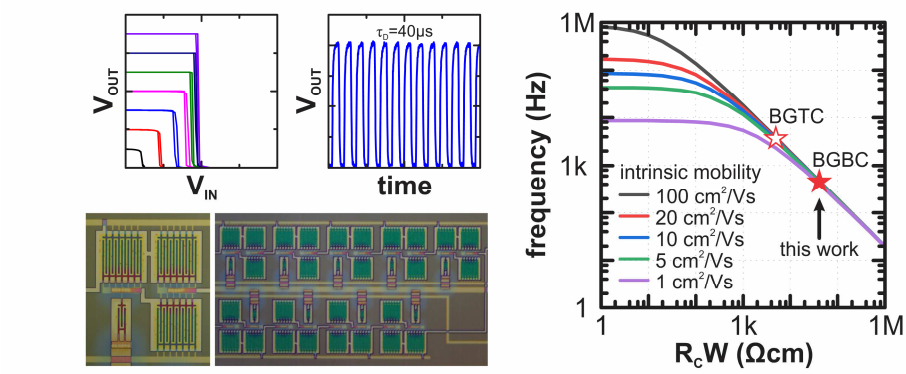
ToC figure (130 mm broad × 50 mm high)



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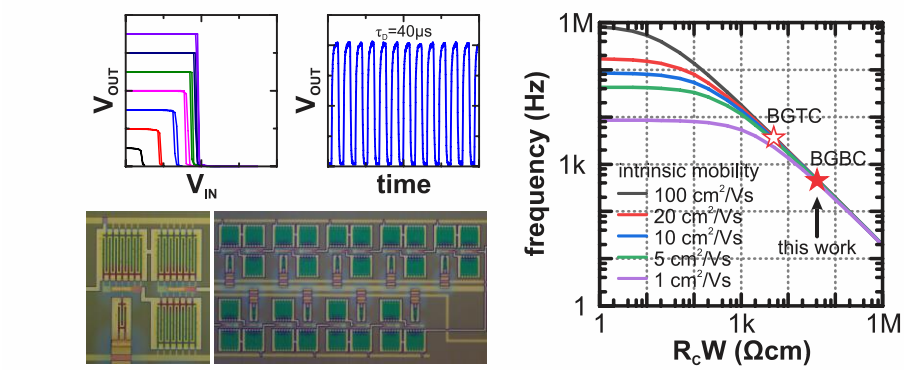

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